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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,889	10/01/2004	Kotaro Takagi	259178US6XPCT	9774
22850	7590	06/16/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			CHEN, JUNPENG	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	
			2631	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/509,889

Applicant(s)

TAKAGI, KOTARO

Examiner

Junpeng Chen

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4, 6-10 and 12 is/are allowed.
- 6) ☒ Claim(s) 5 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 October 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/01/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 371 and 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The information disclosure statement submitted on October 01, 2004 has been considered by the Examiner and made of record in the application file.

### ***Objection - Specification***

3. The disclosure is objected to because of the following informalities:

Each of Figure 1, Figure 2A, Figure 2B, Figure 2C, Figure 3 and Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In line 27 of Page 11, replace "connector" with --collector--

In **line 29 of Page 11**, replace "first" with --second--

In **line 2 of Page 12**, replace "Q11" with --Q9--

In **line 6 of Page 12**, replace "Q9" with --Q11--

In **line 15 of Page 12**, replace "C13" with --C14--

In **line 4 of Page 13**, replace "Q8" with --Q6--

In **line 5 of Page 13**, replace "R13" with --R10--

In **line 6 of Page 13**, replace "P11" with --P12--

In **line 8 of Page 13**, replace "Q6" with --Q8--

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

**Claims 5 and 11** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Consider **Claim 5**, the applicant recites that the emitters of the first differential pair of transistors in the first Gilbert Cell circuit are directly coupled and *selectively*

*connected to [an] own current source and a collector of one of the pair of transistors in the low noise amplifying circuit with the low gain, emitters of the second differential pair of the transistors in the first Gilbert Cell circuit are directly coupled and selectively connected to [an] own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain, emitters of the third differential pair of transistors in the second Gilbert Cell circuit are directly coupled and selectively connected to [an] own current source and a collector of one of the pair of transistors in the low noise amplifying circuit with the low gain, and emitters of the fourth differential pair of the transistors in the second Gilbert Cell circuit are directly coupled and selectively connected to [an] own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain.*

However, according to lines 15-19 on page 17 of the current application, when it is in low gain mode, the terminal B2 is turned off, and the current mirror circuit formed by connecting it to the transistors Q13 to Q16 through the terminal P13 does not operate, so that the four transistors Q13 to Q16 are turned off, and no DC current (read as the own current source as claimed) passes through. In other word, the own current source as claimed was NOT connected to the emitters of each of the differential pair of transistors in the Gilbert Cells when it is in low gain mode.

Therefore, with the disclosed specification, one with ordinary skill in the art would not be enabled to make and/or use the current invention because the specification failed to provide information on how the emitters of each of the differential pair of transistors in

the Gilbert Cells are “*selectively connected* to [their] own current source and [the] collectors of the pair of transistors in the low noise amplifying circuit with low gain”.

Consider **Claim 11**, the applicant recites that the emitters of the first differential pair of transistors in the first Gilbert Cell circuit are directly coupled and *selectively connected to [an] own current source and* a collector of one of the pair of transistors in the low noise amplifying circuit with the low gain, emitters of the second differential pair of the transistors in the first Gilbert Cell circuit are directly coupled and *selectively connected to [an] own current source and* a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain, emitters of the third differential pair of transistors in the second Gilbert Cell circuit are directly coupled and *selectively connected to [an] own current source and* a collector of one of the pair of transistors in the low noise amplifying circuit with the low gain, and emitters of the fourth differential pair of the transistors in the second Gilbert Cell circuit are directly coupled and *selectively connected to [an] own current source and* a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain.

However, according to lines 15-19 on page 17 of the current application, when it is in low gain mode, the terminal B2 is turned off, and the current mirror circuit formed by connecting it to the transistors Q13 to Q16 through the terminal P13 does not operate, so that the four transistors Q13 to Q16 are turned off, and no DC current (read as the own current source as claimed) passes through. In other word, the own current

source as claimed was NOT connected to the emitters of each of the differential pair of transistors in the Gilbert Cells when it is in low gain mode.

Therefore, with the disclosed specification, one with ordinary skill in the art would not be enabled to make and/or use the current invention because the specification failed to provide information on how the emitters of each of the differential pair of transistors in the Gilbert Cells are “*selectively connected* to [their] own current source and [the] collectors of the pair of transistors in the low noise amplifying circuit with low gain”.

Applicant is suggested that by replacing the phrase “selectively connected to said own current source and” with --connected to-- in lines 10-11, 15-16, 23, 27-18 of claim 5 and in lines 11, 15-16, 23 and 27-28 of claim 11 would make claim 5 and claim 11 allowable.

#### ***Allowable Subject Matter***

5. **Claims 1-4, 6-10 and 12** are allowed.

Consider **claims 1-4 and 6**, the best prior art of record found during examination of the present application, Toyoda et al. (U.S. Pub. # 20030119464 A1), discloses a reception circuit that has a low noise amplifier (LNA) 13 connected to a quadrature demodulator 14 and the gain of the low noise amplifier is changeable with the gain control signal from gain control signal generator 23 (paragraph 0027-0028).

However, Toyoda et al. fails to specifically disclose, teach or suggest a quadrature demodulator connected with a *serial capacitance to an output of [the] low*

*noise amplifying circuit with the high gain of [the] low noise amplifier and directly connected to an output of said low noise amplifying circuit with the low gain as claimed in the present application.*

Therefore, claims 1-4 and 6 of the present application are considered novel and non-obvious over the prior art and, consequently, are allowed.

Consider **claims 7-10 and 12**, the best prior art of record found during examination of the present application, Toyoda et al. (U.S. Pub. # 20030119464 A1), discloses a reception circuit that has a low noise amplifier (LNA) 13 connected to a quadrature demodulator 14 and the gain of the low noise amplifier is changeable with the gain control signal from gain control signal generator 23 (paragraph 0027-0028). Toyoda et al. further discloses a reception level detecting means (read as Signal intensity detector 20, Fig. 1, paragraph 0027-0028) for detecting a level of a reception signal (read as signal intensity) and a control mean (read as the combination of Gain selector 21, Timing controller 22 and Gain control signal generator 23, Fig. 1, paragraph 0027-0028) to control the gain of the LNA 13 according to the reception level (read as signal intensity).

However, Toyoda et al. fails to specifically disclose, teach or suggest a quadrature demodulator connected with a *serial capacitance to an output of [the] low noise amplifying circuit with the high gain of [the] low noise amplifier and directly connected to an output of said low noise amplifying circuit with the low gain as claimed in the present application.*



Therefore, claims 7-10 and 12 of the present application are considered novel and non-obvious over the prior art and, consequently, are allowed.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al.	US 6987966 B1	Adaptive radio transceiver with polyphase calibration
Chien	US 20040203472 A1	Compensation of I-Q imbalance in digital transceivers
Jakobsson	US 6757340 B1	Radio receiver and method for preloading an average DC-offset into a channel filter
Matsumoto et al.	US 20040097212 A1	Direct conversion receiver and dc offset reducing method
Hayashi et al.	US 20020094788 A1	Signal processing semiconductor integrated circuit device and wireless communication system
Peterson	US 6073002 A	Mixer circuit and communication device using the same
Baker et al.	US 5724653 A	Radio receiver with DC offset correction circuit

7. Any response to this Office Action should be **faxed to (571) 273-8300 or mailed to:**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Hand-delivered responses** should be brought to

Customer Service Window  
Randolph Building  
401 Dulany Street  
Alexandria, VA 22314


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rafael Perez-Gutierrez can be reached on 571-272-7915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junpeng Chen  
J.C./jc

May 15, 2006

  
RAFAEL PEREZ-GUTIERREZ  
PRIMARY EXAMINER  
6/12/06